U-shaped junction capacitance modelling and **proposal for diode CMC model enhancements**

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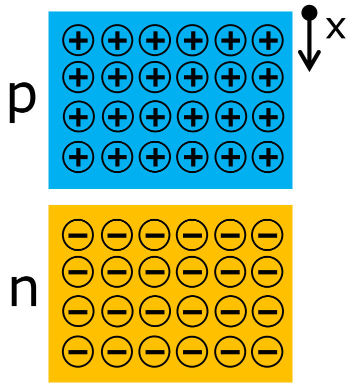
Agenda

U-shaped junction capacitance modelling

Planar (1D) pn junction

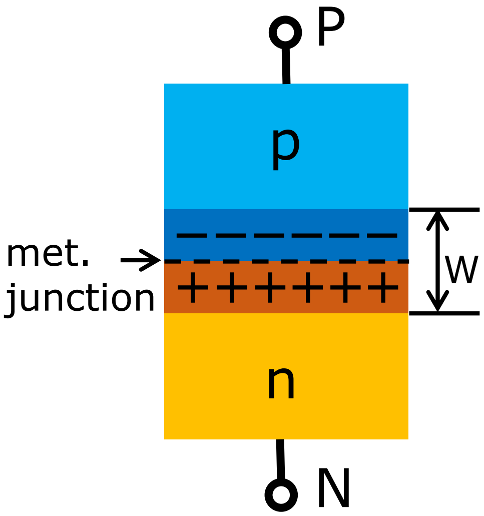
› pn-junction formation
  – Different carrier concentration causes electrons to move to p side of junction
  – Stationary ions are left behind and electric field builds up impeding further exchange until thermodynamic equilibrium is reached

⇒ Space charge region (SCR) is formed



› Applying an external voltage V_{PN}
  – Electric field is changed and carrier exchange is supported/impeded

⇒ SCR-width w is modulated

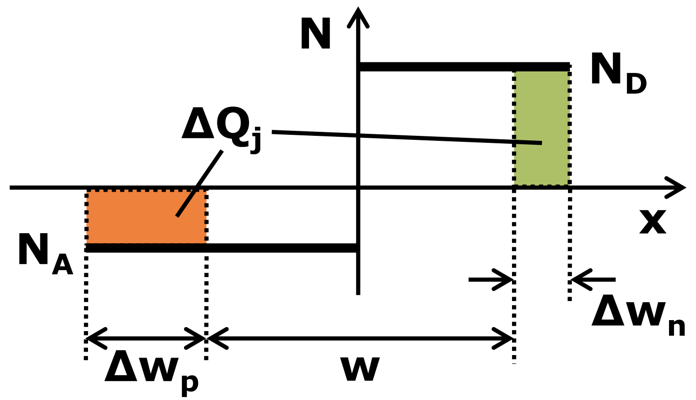


Planar (1D) junction charge

› Poisson equation
  - $\frac{dE}{dx} = \frac{q}{\varepsilon}(N_D - n + N_A + p)$, in SCR $n \approx 0, p \approx 0$
  - Solving the equation for the electric field and potential leads to a linear and quadratic characteristic, respectively

› Width of SCR in thermodynamic equilibrium
  - $w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)[V_d - V_{PN}]}$

› Applying a voltage change ΔV
  - $\Delta Q_j = qN_A\Delta w_p = qN_D\Delta w_n$
  - $= q\frac{N_A N_D}{N_A+N_D}\Delta w$

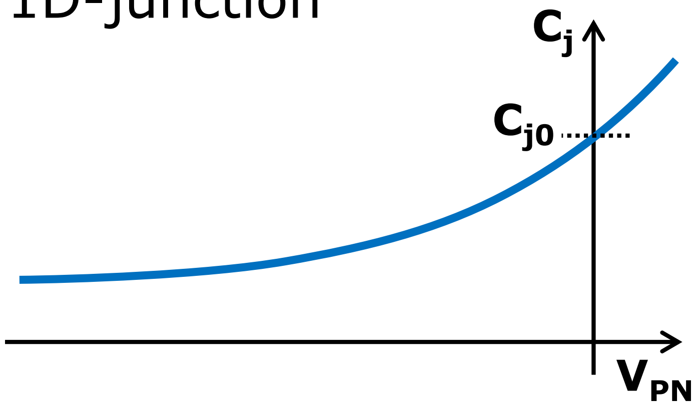


Planar (1D) junction capacitance

› Classical capacitance behaviour of a 1D-junction

– $C_j = \frac{dQ_j}{dV} = q\frac{N_A N_D}{N_A+N_D}\frac{dw}{dV}$

– $= \sqrt{\frac{q\varepsilon}{2[V_d-V_{PN}]}\frac{N_A N_D}{N_A+N_D}} = \frac{C_{j0}}{\left(1-\frac{V_{PN}}{V_d}\right)^{0.5}}$ z



› Generalization of equation

– Three parameters that exist in every compact model with a pn depletion capacitance description

– C_{j0}, V_d, z

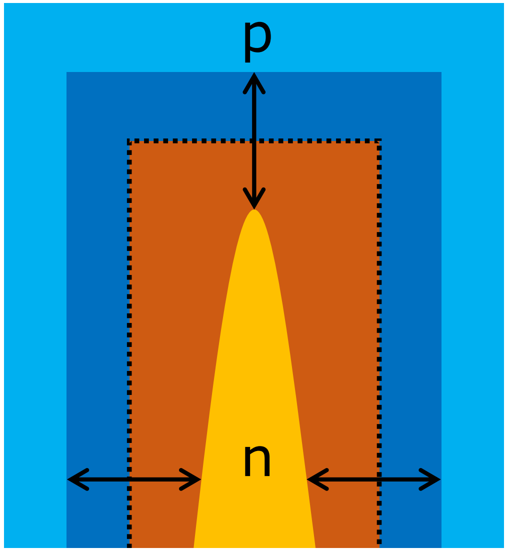
– When V_{PN} approaches V_d, $C_j \rightarrow \infty$

– Derivation of capacitance is not valid for strong forward bias

– E.g. limit C_j to 2*C_{j0} for compact model implementation by smoothing function

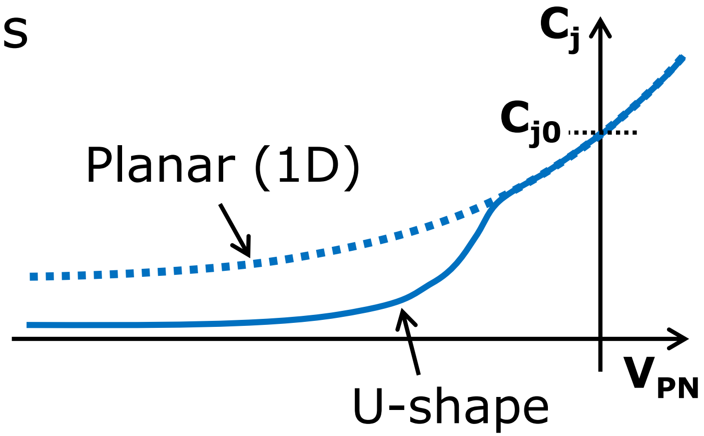
U-shaped junction

- Structure definition
  - n doped region embedded in p body
  - Typically exists similarly in LDMOS devices



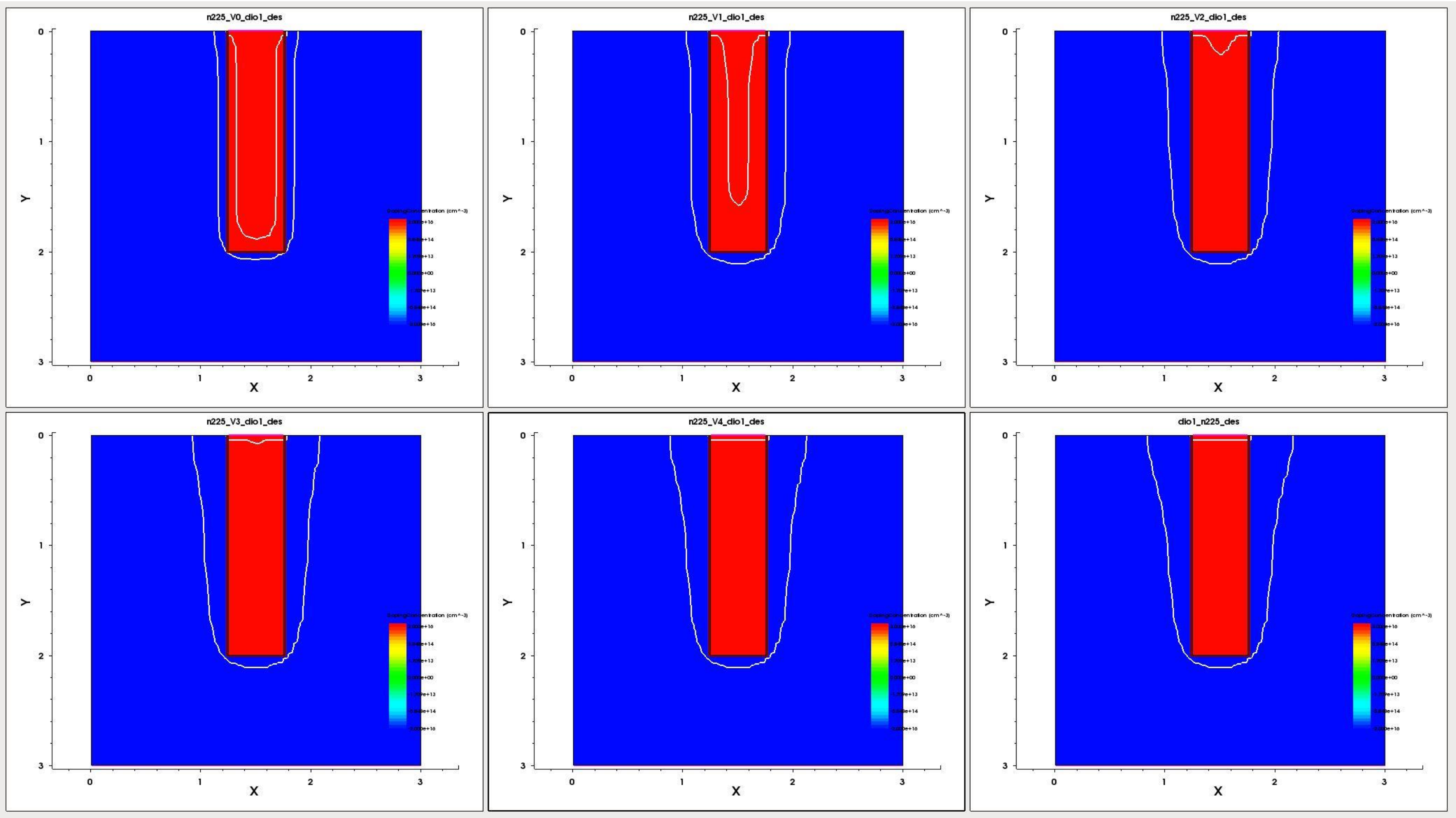
- Capacitance characteristics
  - For positive or slightly negative junction bias, the capacitance is identical to 1D behavior
  - For higher negative bias, SCR grows into n region until full depletion

⇒ Abrupt capacitance drop



TCAD Analysis

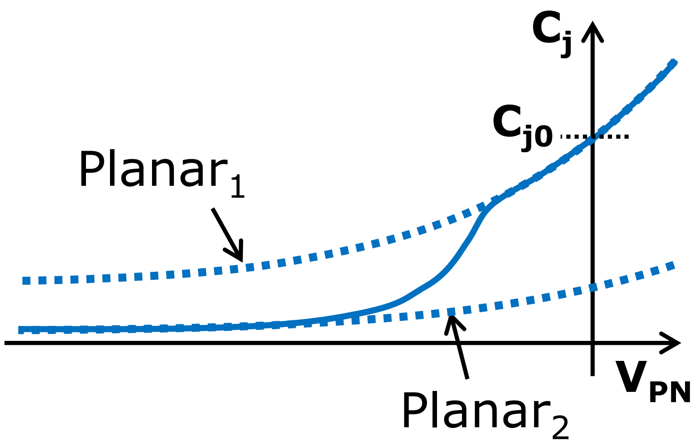
- Simulation results for an exemplary structure (V_{PN} = 0 … -5 V)



Modeling Approach

- Possible solutions
  - Table model: to be avoided due to numerics, limited range, temperature dependence, etc.
  - Complete analytic solution is too complex – involving partial differential equations
- The engineering approach
  - Use two superimposed 1D junction descriptions
  - Apply appropriate transition between each of the descriptions

$\Rightarrow$ Doubles the amount of parameters + parameters for transition

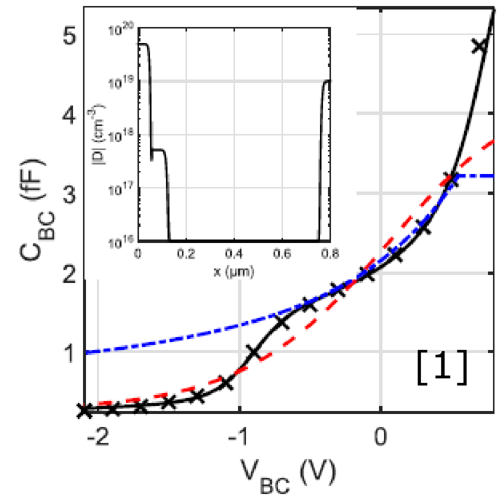


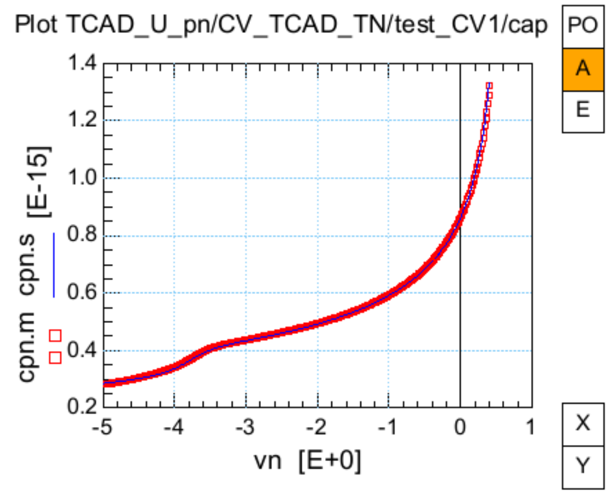
Implementation based on [1]

› Paper [1] analyzes C_{BC} of III/V HBTs
  – Additional doping steps in the collector lead to steps in CV curve
  – Presented characteristics are identical to U-shaped junction
  – Approach smooths between several depletion capacitance descriptions

⇒ Show demo of prototype implementation

› Excellent agreement for TCAD data ☺



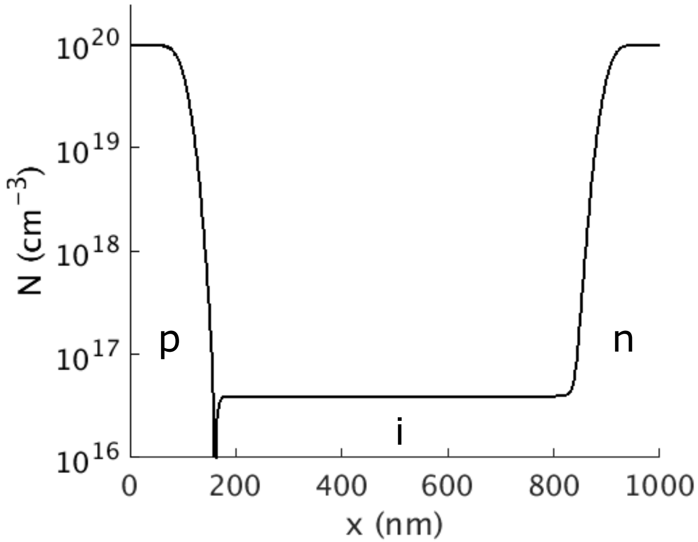


[1] Tobias Nardmann, Michael Schroter and Paulius Sakalas, „A Multiregion Approach to Modeling the Base-Collector Junction Capacitance“, in IEEE Transactions on Electron Devices

Proposal for diode CMC model extension

TCAD analysis of an exemplary pin diode

- Doping profile overview
  - Highly doped p and n at contacts
  - Mildly doped n intrinsic zone
  - Total device length: 1um



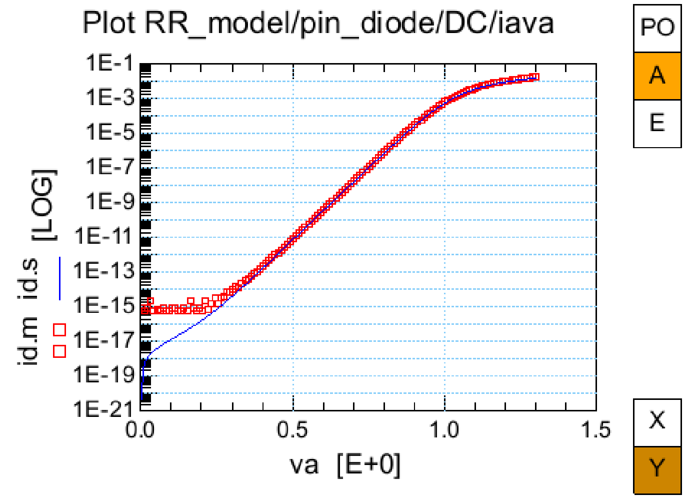
- Full characterization of diode
  - DC & CV simulation
  - Large signal reverse recovery
  - AC simulation

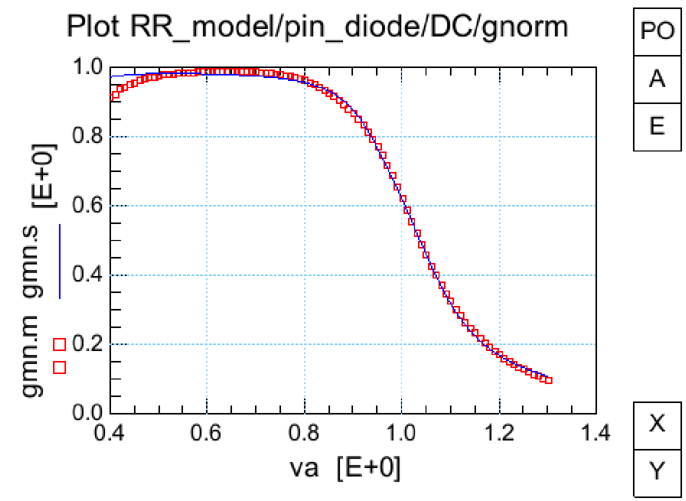
$\Rightarrow$ Comparison with diode CMC compact model

DC simulation results

- Normalized transconductance
  - $I_{PN} = I_S \exp\left[\frac{V_{PN}}{mV_T} - 1\right], g_{PN} = \frac{dI_{PN}}{dV_{PN}}$
  - $g_{norm} = g_{PN}/I_{PN}V_T \approx 1$ (at low inj.)
- Forward bias DC
  - Match low injection by emission coefficient and saturation current
  - High injection matched by diodeCMC model and series resistance

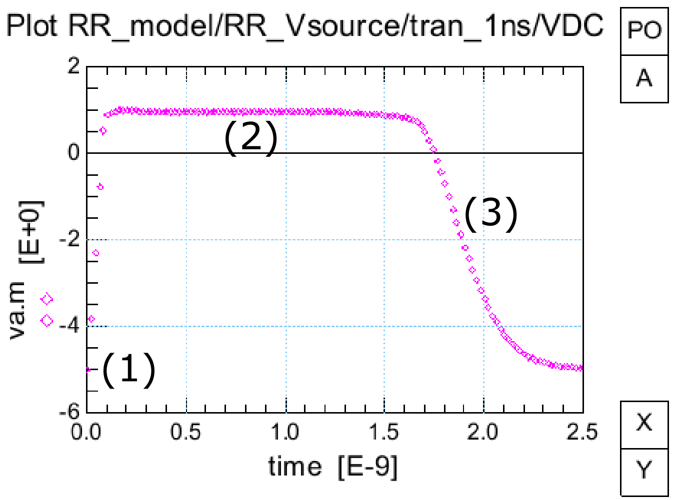
⇒ Model accuracy is very good (~4% error)

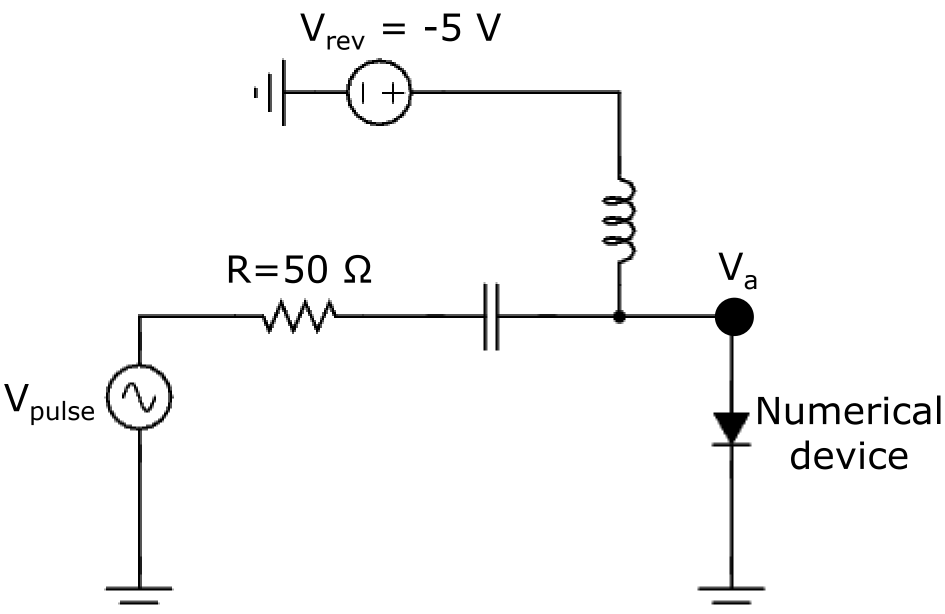




Reverse recovery overview

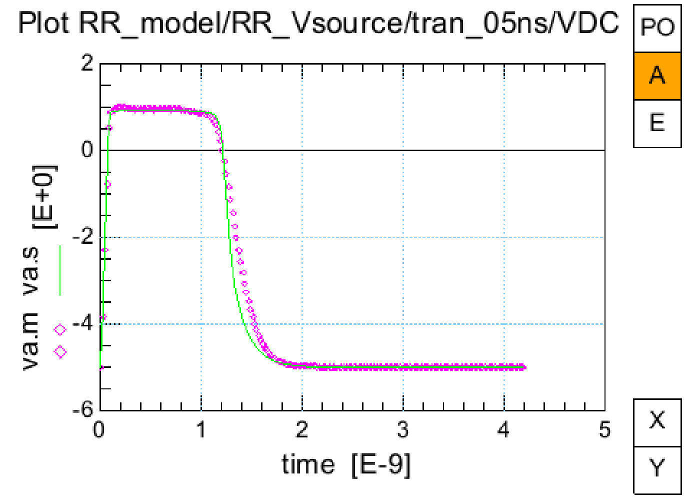
- Mixed mode (numerical device + circuit) simulation
- Reverse recovery sequence
  - Device is reverse biased initially, voltage pulse is applied (1)
  - Device is then forward biased for a certain time (2)
  - After positive pulse is over, device goes into recovery (3)

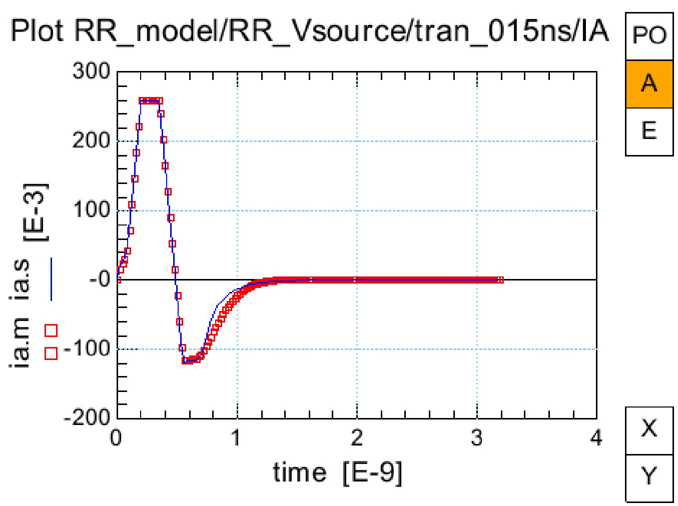


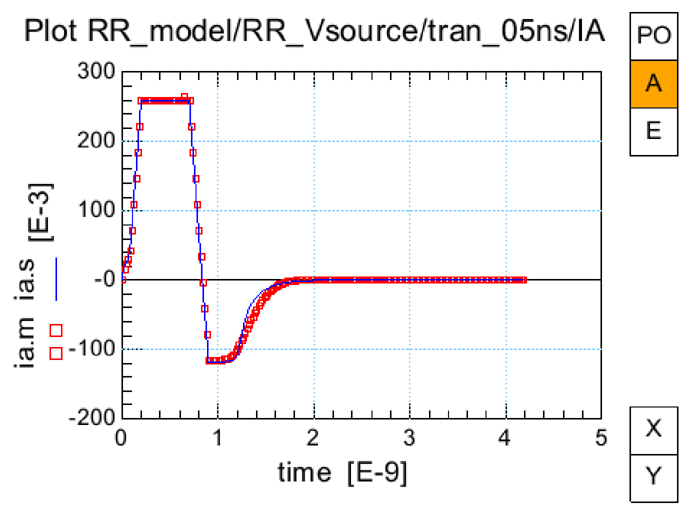


Reverse recovery simulation results

- Prerequisite:
  DC and dep. capacitance modelling
- Good agreement between model and TCAD
  - Some discrepancies for shorter pulse widths

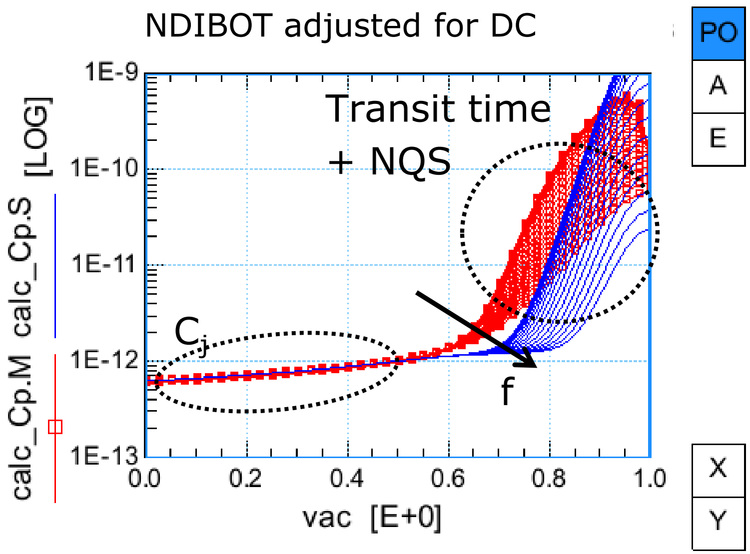


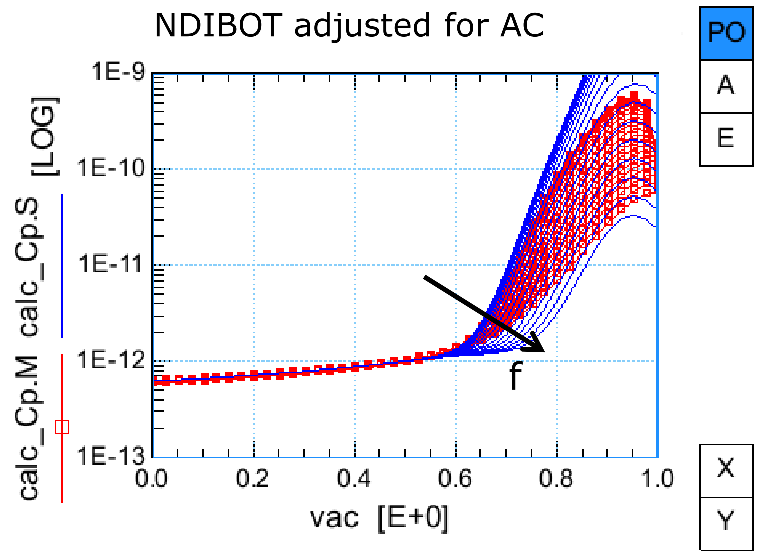




AC simulation results

› Small-signal pin diode capacitance + (transit time)





› lhs: NDIBOT adjusted for correct onset of high injection (DC)

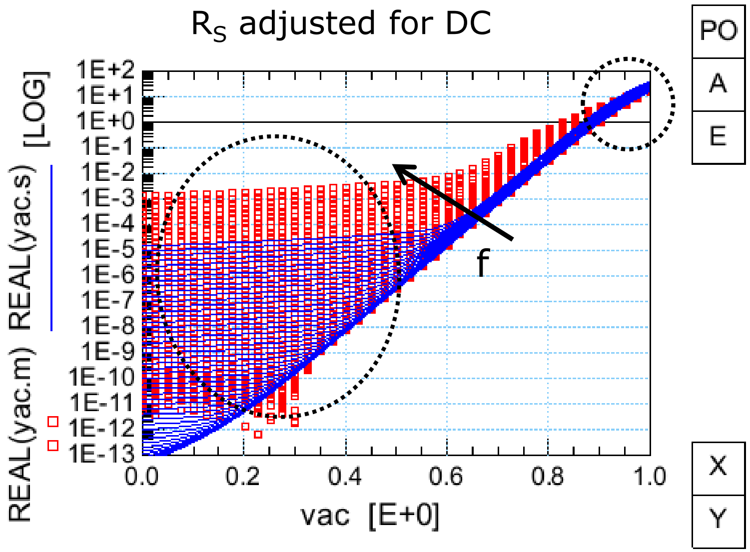
› rhs: NDIBOT adjusted for correct onset of high injection (AC)

⇒ Decouple behavior by introducing additional parameter

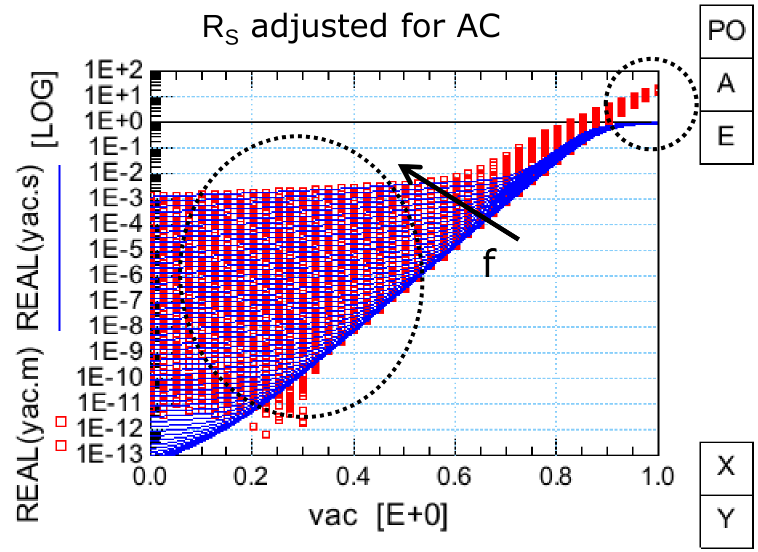
AC simulation results

› Small-signal pin diode conductance

R_S adjusted for DC



R_S adjusted for AC



› lhs: series resistance adjusted for high injection (DC)

› rhs: series resistance adjusted for low injection (AC)

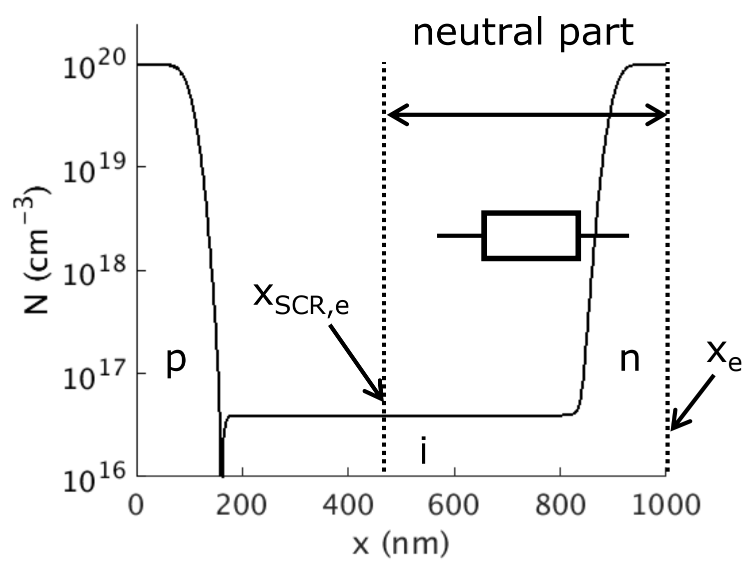
⇒ Need advanced model for series resistance (it's bias dependent!)

Series resistance overview

› Characteristics of resistance
  - Main contribution to R_S is the neutral part of the intrinsic zone
  - Low injection: SCR width depends on applied voltage

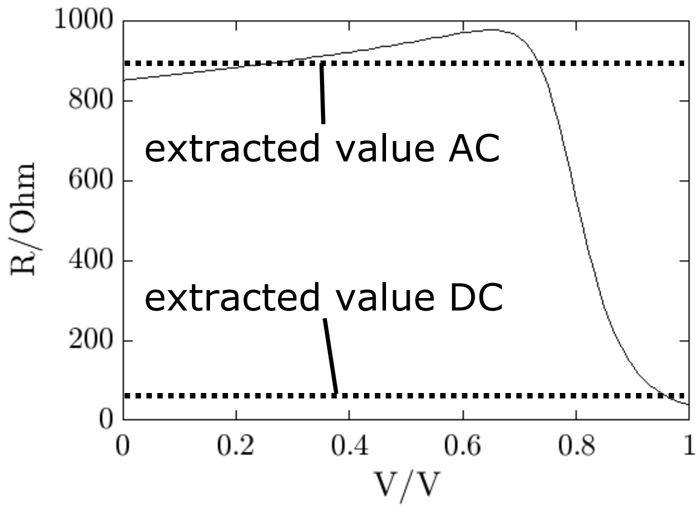
  ⇒ Resistance modulation
  - High injection: intrinsic zone is flooded with holes

  ⇒ Series resistance drops to extracted DC value



TCAD evaluations for series resistance

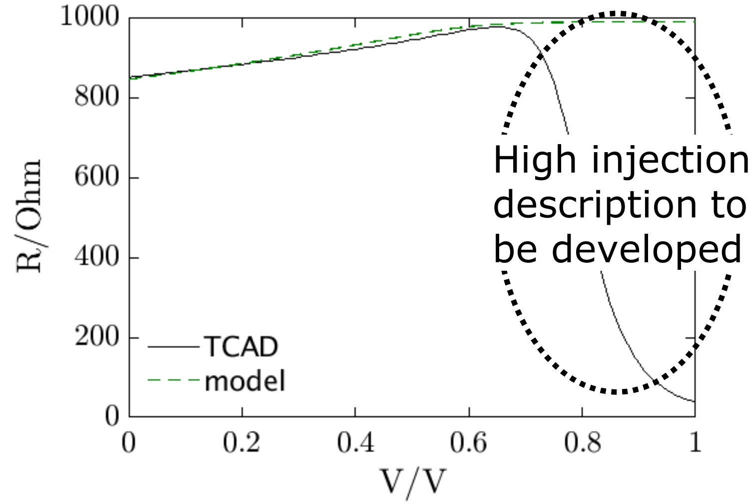
- Calculation from TCAD
  - $R_S = \int_{x_{SCR,e}}^{x_e} \frac{1}{q(n\mu_n + p\mu_p)} dx$
  - Unit of R_S: $[R_S] = \Omega m^2$
  - Divided by area of diode gives resistance for specific device



- Diode CMC model extension
  - Resistance modulation can be modelled by change of junction capacitance
    - Accurate physics-based prototype solution already implemented in .va code ☺
  - Physics-based description for high injection to be developed

Series resistance: voltage dependent portion

- Model derivation
  - $R_S = \int_{x_{SCR,e}}^{x_e} \frac{1}{q(n\mu_n + p\mu_p)} dx$
  - $R_S \approx \frac{1}{q\bar{n}_{epi}\bar{\mu}_{epi}} [x_e - x_{SCR,e}]$
  - $R_{S0} = R_S(V=0) \approx \frac{1}{q\bar{n}_{epi}\bar{\mu}_{epi}} [x_e - x_{SCR,e0}]$
  - The doping in the intrinsic region is low ($N_A \gg N_D$)
    - We can assume that the SCR width in the p region is negligible ($w \approx x_{SCR,e}$, $w_0 \approx x_{SCR,e0}$)
    - We can assume that the resistance contribution at the highly doped n side is small ($x_e \approx W_I$, parameter already exists in dioCMC)
    - $R_S = R_{S0} \frac{x_e - x_{SCR,e}}{x_e - x_{SCR,e0}} \approx R_{S0} \frac{W_I - w}{W_I - w_0}$
    - Calculate w based on $w = \frac{\varepsilon A}{C_j}$ and insert into equation for R_S



Conclusion

- U-shaped junction capacitance overview
  - Multi-region capacitance model [1] applied successfully

- Diode CMC model extension proposals
  - Decouple AC from DC behavior by introducing NDIBOTAC & NDIBOTDC
  - Implement advanced series resistance formulation
    - Prototype implementation for resistance modulation component (voltage dependent) already working
    - Current dependent resistance drop yet to be modelled
  - Implement two region junction capacitance model based on [1]

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